

Appl. No. 10/690,655  
Amdt. dated 4/4/06  
Reply to Office Action of 11/3/05

PATENT  
Docket: 020548

IN THE CLAIMS:

1. (Currently amended) A programmable dynamic range receiver, comprising:  
a jammer detector for detecting the presence of jamming in an RF signal; and  
a state machine controlling the receiver based on the results of the jammer detector  
detecting the presence of jamming in the RF signal, the state machine operative to transition the receiver between a plurality of states, said states including at least one state corresponding to a high linearity receiving mode and at least one state corresponding to a low linearity receiving mode,  
wherein the state machine is operative to enter a state corresponding to the high linearity receiving mode faster than entering a state corresponding to the low linearity receiving mode and operative to leave a state corresponding to the high linearity receiving mode slower than leaving a state corresponding to the low linearity receiving mode.
2. (Currently amended) The programmable dynamic range receiver of the Claim 1,  
further comprising:  
an amplifier being coupled or integral to the jammer detector.
3. (Original) The programmable dynamic range receiver of Claim 1, further comprising:  
an RF bandpass filter electronically connected to the output of the LNA;  
a mixer coupled to the output of the RF bandpass filter;  
an oscillator coupled to the mixer;  
a low pass filter coupled to the mixer; and  
the jammer detector coupled to the output of the mixer before the input of the low pass filter.
4. (Original) The programmable dynamic range receiver of Claim 1, further comprising:  
a comparator coupled to the jammer detector for detecting the level of jamming in the RF signal.
5. (Original) The programmable dynamic range receiver of Claim 1, further comprising:

Appl. No. 10/690,655  
Amdt. dated 4/4/06  
Reply to Office Action of 11/3/05

PATENT  
Docket: 020548

a multi-bit Analog-to-Digital converter (ADC) coupled to the jammer detector for detecting the level of jamming in the RF signal.

6. (Original) The programmable dynamic range receiver of Claim 1, further comprising: an attenuator coupled to the input of the jammer detector to prevent leaking of the interference back to the signal path.

7. (Original) The programmable dynamic range receiver of Claim 1, further comprising: means for interfacing the state machine with the jammer detector.

8. (Original) The programmable dynamic range receiver of Claim 1, wherein the state machine utilizes a FFT calculation to determine jamming in an RF signal.

9. (Original) The programmable dynamic range receiver of Claim 1, further comprising: a power control, including an up bit counter to adjust the gain in the receiver, the up bit counter results being reported to the state machine for controlling the receiver based on an average of up bits.

10. (Original) The programmable dynamic range receiver of Claim 9, further comprising:

a timer for providing temporal hysteresis between high and low power consumption modes based on a combination of average number of up bits counted in a period of time or the presence of jamming in the RF signal.

11. (Original) The programmable dynamic range receiver of Claim 1, further comprising:

an analog to digital converter being coupled the output of a mixer, wherein an analog to digital converter goes to fewer number of effective bits if the total interference in the channel is less than a predetermined threshold.

Appl. No. 10/690,655

Amdt. dated 4/4/06

Reply to Office Action of 11/3/05

PATENT

Docket: 020548

12. (Original) The programmable dynamic range receiver of Claim 1, wherein the state machine comprises logic circuitry.

13. (Original) The programmable dynamic range receiver of Claim 1, wherein the state machine controls the receiver by software, hardware, or a combination of software and hardware.

14. (Original) The programmable dynamic range receiver of Claim 1, wherein the state machine controls the receiver by adjusting, switching, parsing, biasing, turning on or off, or otherwise manipulating components of the receiver or system.

15. (Currently amended) A programmable dynamic range receiver, comprising:  
a power control component, including an up bit counter to adjust the gain in the receiver, the up bit counter results being reported to a state machine for controlling the receiver based on an average of up bits, the state machine operative to transition the receiver between a plurality of states, said states including at least one state corresponding to a high linearity receiving mode and at least one state corresponding to a low linearity receiving mode,

wherein the state machine is operative to enter a state corresponding to the high linearity receiving mode faster than entering a state corresponding to the low linearity receiving mode and operative to leave a state corresponding to the high linearity receiving mode slower than leaving a state corresponding to the low linearity receiving mode.

16. (Currently amended) A method of providing programmable linearity in a receiver, comprising:

detecting the presence of jamming in the RF signal; and

controlling the receiver based on the results of the detecting step indicating the presence of jamming in the RF signal, said controlling performed by a state machine operative to transition the receiver between a plurality of states, said states including at least one state corresponding to a high linearity receiving mode and at least one state corresponding to a low linearity receiving mode,

Appl. No. 10/690,655  
Amdt. dated 4/4/06  
Reply to Office Action of 11/3/05

PATENT  
Docket: 020548

wherein the state machine is operative to enter a state corresponding to the high linearity receiving mode faster than entering a state corresponding to the low linearity receiving mode and operative to leave a state corresponding to the high linearity receiving mode slower than leaving a state corresponding to the low linearity receiving mode.

17. (Original) The method of Claim 16, further comprising:  
providing the results of the detecting step indicating the presence of the jamming in the RF signal step to a component in the receiver.

18. (Canceled)

19. (Canceled)

20. (Original) The method of Claim 16, further comprising:  
providing a filter to reject band jammers.

21. (Original) The method of Claim 18, wherein the state machine controls the low-noise amplifier based on the results of detecting the presence of jamming in the RF signal so as to lower the power consumption of the programmable receiver when jamming is not present in the RF signal.

22. (Original) The method of Claim 16, further comprising:  
after detecting the presence of jamming in the RF signal, measuring the amount of jamming in the RF signal;  
comparing the amount of jamming in the RF signal versus a threshold amount; and  
providing the results of the measured amount of jamming in the RF signal step to the receiver.

23. (Original) The method of Claim 16, further comprising:  
providing temporal hysteresis to the receiver depending upon the results of the step of detecting the presence of jamming in the RF signal.

Appl. No. 10/690,655  
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Docket: 020548

24. (Original) The method of Claim 16, further comprising the step of:  
providing means for determining a carrier-to-noise ratio for detecting the presence of jamming in the RF signal.

25. (Original) The method of Claim 24, further comprising the step of:  
utilizing the means for determining the carrier-to-noise ratio to count the number of up bits in a time period to detect the presence of jamming in the RF signal.

26. (Original) The method of Claim 16, further comprising the step of:  
providing an analog to digital converter being coupled to the output of a mixer, wherein the analog to digital converter goes to fewer bits if the total interference in the channel is less than a predetermined threshold.

27. (Currently amended) An integrated chip (IC) for providing programmable linearity in a receiver, comprising:

a jammer detector for detecting the presence of jamming in an RF signal; and  
a state machine controlling the receiver based on the results of the jammer detector  
detecting the presence of jamming in the RF signal, the state machine operative to transition the receiver between a plurality of states, said states including at least one state corresponding to a high linearity receiving mode and at least one state corresponding to a low linearity receiving mode.

wherein the state machine is operative to enter a state corresponding to the high linearity receiving mode faster than entering a state corresponding to the low linearity receiving mode and operative to leave a state corresponding to the high linearity receiving mode slower than leaving a state corresponding to the low linearity receiving mode.

28. (Original) The integrated chip of Claim 27, wherein the integrated chip is an RF chip.

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PATENT  
Docket: 020548

29. (Currently amended) An integrated chip (IC) for providing programmable linearity in a receiver, comprising:

means for detecting the presence of jamming in the RF signal; and

state machine means for controlling the receiver based on the results received from the means for detecting indicating the presence of jamming in the RF signal, the state machine means operative to transition the receiver between a plurality of states, said states including at least one state corresponding to a high linearity receiving mode and at least one state corresponding to a low linearity receiving mode.

wherein the state machine means is operative to enter a state corresponding to the high linearity receiving mode faster than entering a state corresponding to the low linearity receiving mode and operative to leave a state corresponding to the high linearity receiving mode slower than leaving a state corresponding to the low linearity receiving mode.

30. (Original) The integrated chip of Claim 29, wherein the integrated chip is an RF chip.